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PROCEEDINGS

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Enhancing Education Quality
In Facing Asian Community

Management and Governance

Quality Assurance

Teaching and Learning

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PREFACE

In line with the development of human civilization, competition has become one of the central issues arising among countries. It demands the nations to have goods and services of good quality. The quality of goods and services provided by a nation depend on the quality of the human resources. Furthermore, the quality of the human resources depends much on the quality of education of the nation. Therefore, the demand on the education quality is reasonably true. The fact shows that only qualified education can produce qualified human resources; and only qualified human resources can produce goods and services of good quality for regional as well as international market. In addition, quality education can only be obtained through a learning process of good quality, good management of quality education, good education quality assurance, research by qualified faculty, and other factors.

Referring to those facts, the Postgraduate Program of University of PGRI Semarang Indonesia hosts an interdisciplinary International Conference on the exploration of a broad range of Educational Quality themes focusing on the quality enhancement of: 1) education management, 2) teaching-learning process, 3) education quality assurance, and 4) the quality of education research.

The conference is hopefully can be a forum for exchanging ideas and research outcomes and for addressing challenges to the vision of an integrated ASEAN Community in relation to the quality of higher education, particularly for academics and students, scholars, experts, and researchers.

On behalf of the Committee, I would like to express our heartfelt thanks to Mr. Mark Heyward, Ph.D. (Australia), Ms. Sopantini, Ph.D. (Australia), Prof. Dr. Sugiyono, M.Pd. (Indonesia), and Mr. Manish Semwal, Ph.D (India) for their incredible contribution as the key speakers. Our gratitude also goes to Rector of University of PGRI Semarang for all the facilities provided, with which the conference runs well. Special thanks go as well to all the presenters and participants without whom this conference may not run. To anyone contributing and participating, I wish that we will have a very productive and successful conference for the betterment of education quality.

Semarang, May 30, 2015.
Chair of OC,

Dr. Ngasbun Egar, S.Pd., M.Pd.
Deputy Director of Post Graduate Program
University of PGRI Semarang

WELCOMING SPEECH

Dear Speakers, Esteemed guests, participants, Ladies and gentlemen,

We are delighted and honored to host this conference on Enhancing Education Quality in facing Asian Community. I am very pleased to welcome you to University of PGRI Semarang and to this conference. I wish for you an enjoyable and productive stay in our beautiful capital city of Central Java.

Your presence here this morning at this international conference emphasizes important aspects of the quality of education especially focusing on education management, teaching learning process, education quality assurance, and researches in education. I am confident that the conference will stimulate discussion about issues of common concern in the field of quality education. By the end of our sessions, I believe that we will be able to identify benefits of our work together that will apply individually and collectively to educational practices in our contexts.

Ladies and Gentlemen, we, Post Graduate Program of the University of PGRI Semarang, take special interest in this conference for at least two reasons: Firstly, the focus of the conference is education, a process that is at the heart of the development of our country. The quality of education will depends much on the quality of the management, teaching-learning process, researches, as well as the quality assurance, beside other important aspects. Secondly, this is an international conference. Conferences such as this give us an opportunity to sift through international ideas and to choose those which can be adapted to improve our national institutions. International discussions allow us to make our contributions to the major world-wide issues of the day as well and thus to establish our place among the nations of the world. The substance of the various sessions of this conference and the expertise of the plenary and parallel presenters and other participants will provide us with excellent opportunities both to give and to receive from the international dialogue.

Finally, I take this opportunity to express my hope that this conference will be an important step in our efforts to improve the quality of education everywhere. I wish you all the success in your efforts.

Once again, let me welcome you to University of PGRI Semarang. We look forward to learning about your discussions and deliberations. I should note that the Post Graduate Program of University of PGRI Semarang has been in the efforts of developing an effective education which is under constant assessment and improvement. This conference should help us in our endeavors to expand and improve.

Semarang, May 30, 2015.
Chair of SC,

Prof. Dr. Sunandar, M.Pd.
Director of Post Graduate Program
University of PGRI Semarang

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DIGITAL CIRCUIT DESIGN AND SIMULATION OF COMBINATION FOR CONTROLLING PUMP ELECTRIC MOTORS HYDRANT WITH ZELIO SOFT 2

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ABSTRACT

Digital circuit is a combination of a digital chain of the output is only dependent on the input current and is independent of input or output earlier. The method is often used to design digital circuits are combined using boolean algebra or Karnaugh map. Zelio Soft 2 software is derived from the company Schneider Electric that are used to create a PLC program (Programmable Logic Controller). Zelio Soft 2 has two models in making the program, which uses ladder diagram (LD) and fuction Block (FBD). If in making a program using FBD then we use a lot of logic gate elements, such as a full adder, multiplexer, decoder, standard logic gates. From the results of the design shows that the Zelio soft 2 makes it easy to analyze digital circuit combination. In addition to simulating the design of digital circuits can be implemented using any combination of Zelio logic.

Keywords: *Zelio Soft 2, Full Adder, Multiplexer*

Introduction

Digital circuit or logic circuit is a circuit composed of passive electronic components and active electronics that make up a digital signal processing function, for example operation number system, multiplexer, encoding, decoding. Logic element is a union of passive and active components in a digital circuit. Forms the smallest logic elements are logic gates (logic gate) which serves to perform logical operations such as OR, AND, and NOT. Prior to the IC (integrated circuit) digital circuits, logic gates implemented or prepared using passive and active electronic components separate (discrete).

Figure 1.1 Digital circuit

In accordance with the development of electronics, especially semiconductor components, then share the type of logic gate has been made in the form of IC. Digital circuit is a combination of a digital chain of the output is only dependent on the input current and is

independent of input or output earlier. The method is often used to design digital circuits are combined using boolean algebra or Karnaugh map.

Zelio Soft 2 software is derived from the company Schneider Electric that are used to create a PLC program (Programmable Logic Controller). Zelio Soft 2 has two models in making the program, which uses ladder diagram (LD) and fuction Block (FBD). If in making a program using FBD then we use a lot of logic gate elements, such as a full adder, multiplexer, decoder, standard logic gates.

Basic Theory

a. Adder Circuit[3]

Binary adder circuit is a digital circuit that functions to perform binary addition operation. The sum of 1-bit binary number can be Half or Full Adder Adder. Half Adder is a summing circuit which ignores the rest of the sum in advance at the input, while the Full Adder is a summing circuit that inserts rest of the sum in advance at the input.

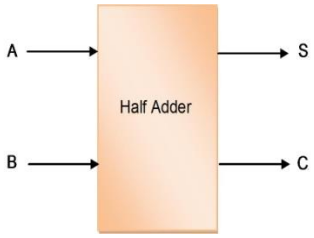


Figure 2.1 Half Adder

Table 2.1 Truth table half adder

INPUT		OUTPUT	
A	**B**	**S (Sum)**	**C (Carry)**
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Based on Table 2.1 can be implemented by using a string of Half Adder logic gate NAND, NOR, EX-OR or in the form of SOP and POS. From the picture logic circuit can be determined equation S (sum) and C (carry).

$S = \overline{A}.B + A.\overline{B} = A \oplus B$

$C = A.B$

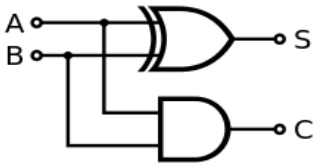


Figure 2.2 Half Adder circuit

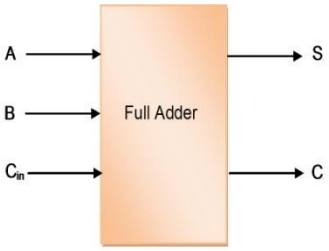


Figure 2.3 Full Adder

Table 2.2 Truth table Full Adder

INPUT			OUTPUT	
A	**B**	**Cin**	**S**	**Cout**
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

A Full Adder add two binary numbers and each bit in the same position for aggregated. Full Adder summing two input bits plus the residual value of the sum (carry-out) from the sum of the previous bit. The output of the Full Adder is the sum (Sum) and the remaining bits (carry-out). Based on Table 2.2 can be made full adder logic circuit using the EX-OR gate.

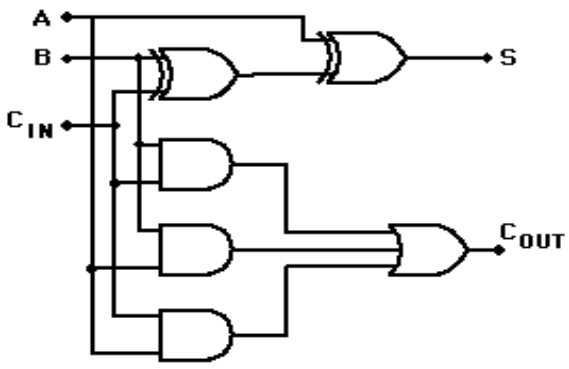


Figure 2.4 Full Adder logic circuit

Full output equation adder logic circuit shown in Figure 2.4 is

$S = A \oplus B \oplus C_{in}$

$C_{out} = A.B + A.C_{in} + B.C_{in}$

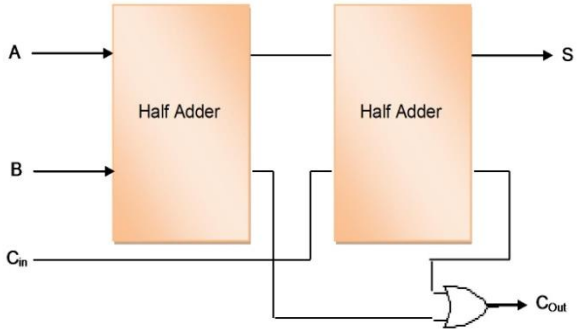


Figure 2.5 Full Adder using two Half Adder

b. Multiplexer and Demultiplexer[3]

Multiplexer (MUX) is a logic circuit that functions to select multiple data input and only the data contained in the output. In the process of selection of data is done with the help of voters or control signals, so the multiplexer can also be referred to as the voter data.

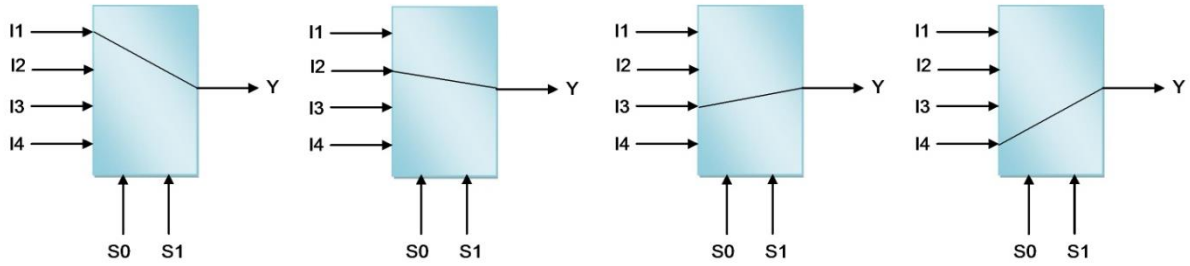


Figure 2.6 Working system Multiplexer

On Figure 2.6 shows the process of selecting the data of the data I1 to I4 and the data is only one data out on Y.

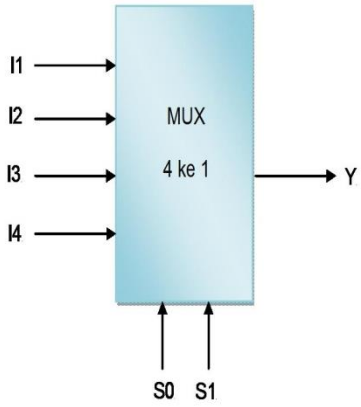


Figure 2.7 MUX 4 to 1

A multiplexer (MUX) 4 to 1 has four input data and the output data is shown in Table 2.3.

Table 2.3 Truth table MUX 4 to 1

SELECTOR		OUTPUT
S1	S0	Y
0	0	I1
0	1	I2
1	0	I3
1	1	I4

Demultiplexer (Demux) which is the opposite of the multiplexer serves to channel the input data to one of several output signals with the help of the voters, so that the demultiplexer can be called channeling data.

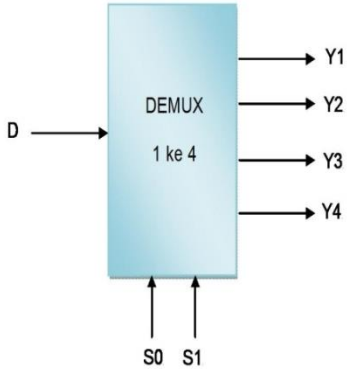


Figure 2.8 Demux 1 to 4

Table 2.4 Truth table DEMUX 1 to 4

SELECTOR		OUTPUT			
S1	S0	Y1	Y2	Y3	Y4
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Demultiplexer of the truth table in Table 2.4 shows the output at Y1 to Y4 and regulated by S1 and S0.

c. Decoder[3]

Decoder is a digital circuit that serves to re-encodes binary code into the original data and the output will be enabled with the possibility of one of the combinations of inputs. Decoder function is the opposite of the encoder, which converts the data input into a binary

code at the output. Several types of decoders are often met decoder 3x8 (3-bit input and 8 output line), 4x16 decoder, decoder BCD to Decimal (4-bit input and 10 output line), BCD to 7 segment decoder (4-bit input and 8 output line).

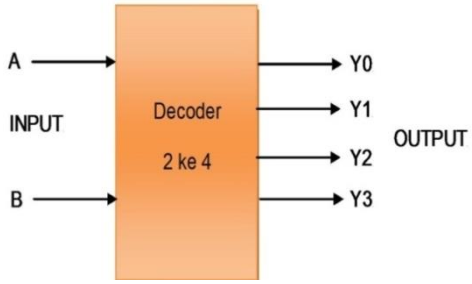


Figure 2.9 Decoder 2 to 4

Table 2.5 Truth table Decoder 2 to 4

INPUT		OUTPUT			
B	A	Y0	Y1	Y2	Y3
0	0	**1**	0	0	0
0	1	0	**1**	0	0
1	0	0	0	**1**	0
1	1	0	0	0	**1**

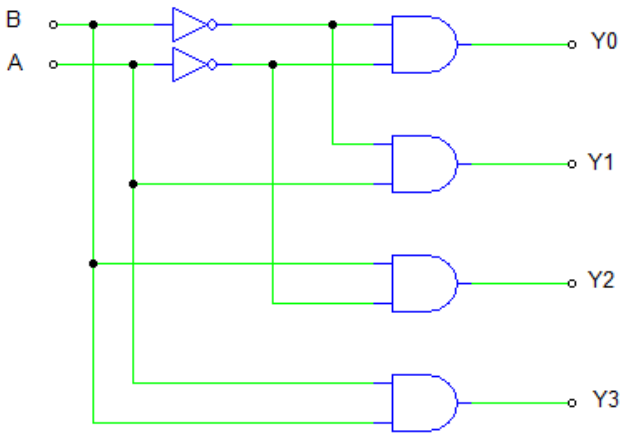


Figure 2.10 Decoder logic circuit

Method

Form of digital circuit design research in the form of a combination of simulation using program Zelio Soft 2. In doing research there are several steps being taken, namely: to design Half and Full Adder Adder, perform design Multiplexer and demultiplexer, decoder design, perform water level controller design, hydrant pump motor controller design. set the input and output variables, and perform simulation of the design.

Results and Discusion

a. Half Adder and Full Adder

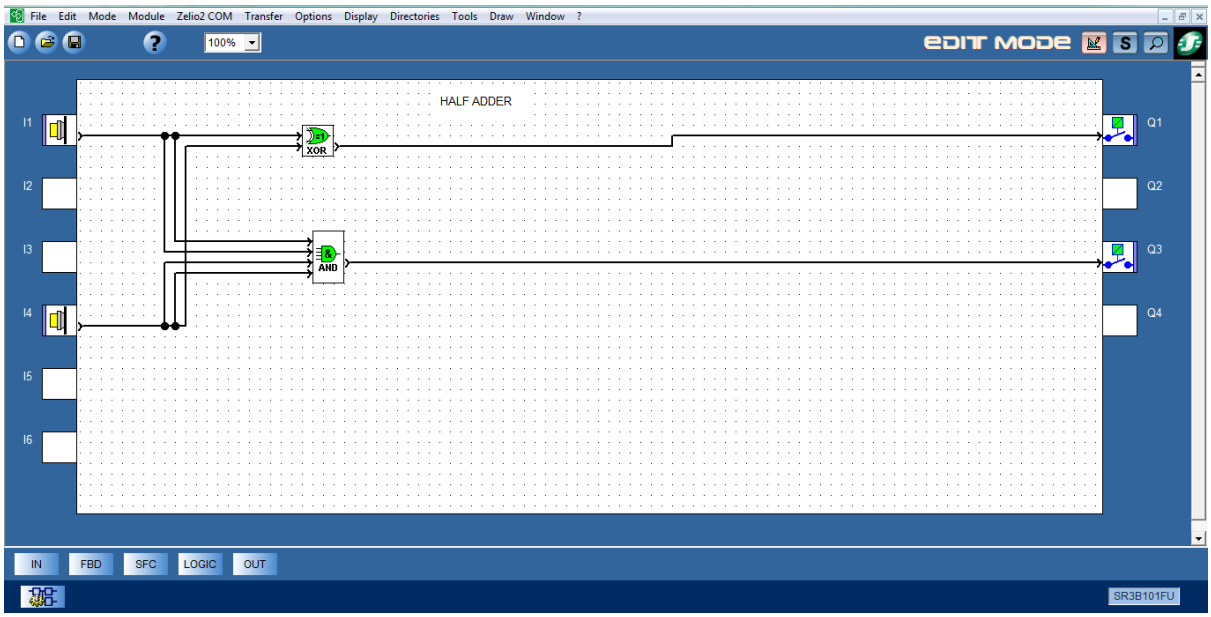


Figure 4.1 Designed by Half Adder

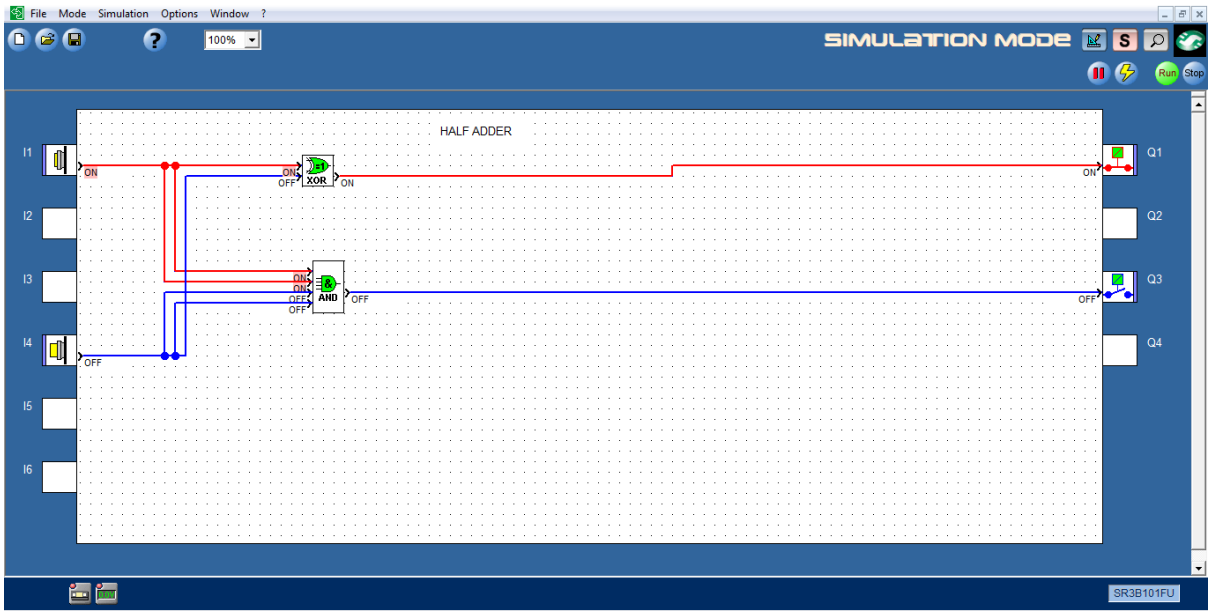


Figure 4.2 Simulation Half Adder

Half Adder design results shown in Figure 4.1, this circuit uses EX-OR gate for output to the output AND Sum and Carry. Input using push button, if the button is pressed, the input provides logic 1 and if the button is released the input provides logic 0. The output using relay contacts, if the relay receives a logic 1 then the relay contacts will close and if the relay receives a logic 0 then the relay contacts will open. Half Adder course of the simulation circuit shown in Figure 4.2.

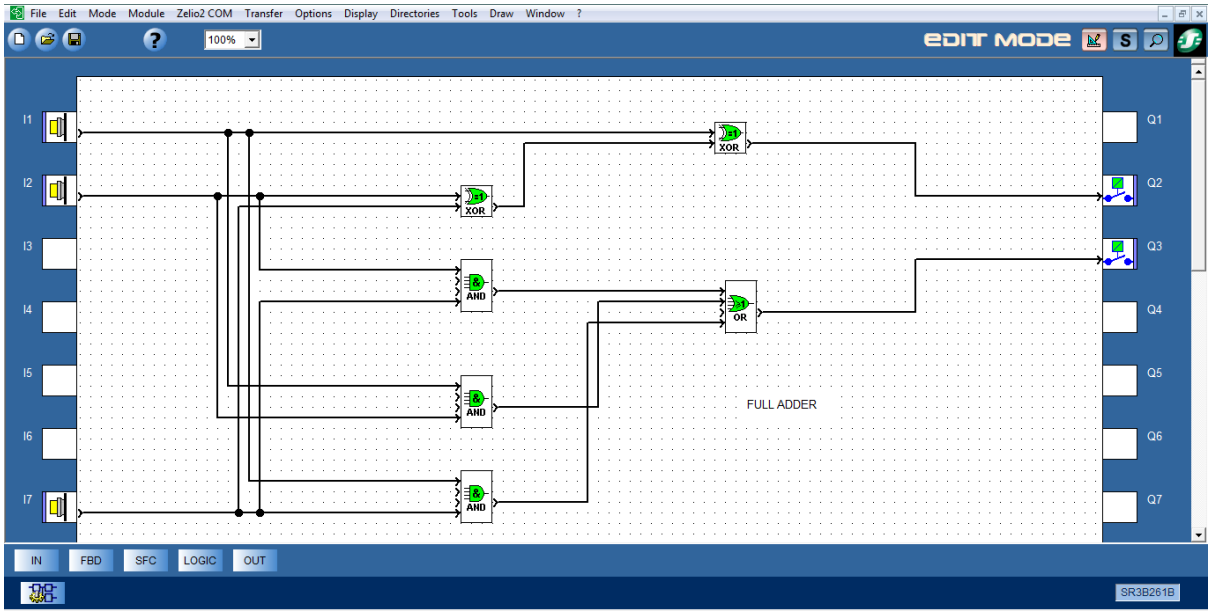


Figure 4.3 Designed by Full Adder

Figure 4.3 is the design of the Full Adder using two EX-OR gates and three AND gates. Input circuit using push button and output relay contacts are also used. In the simulation visible if the push button is pressed or give logic 1 and push button also provides a logic 1, the output relay contacts on both will close.

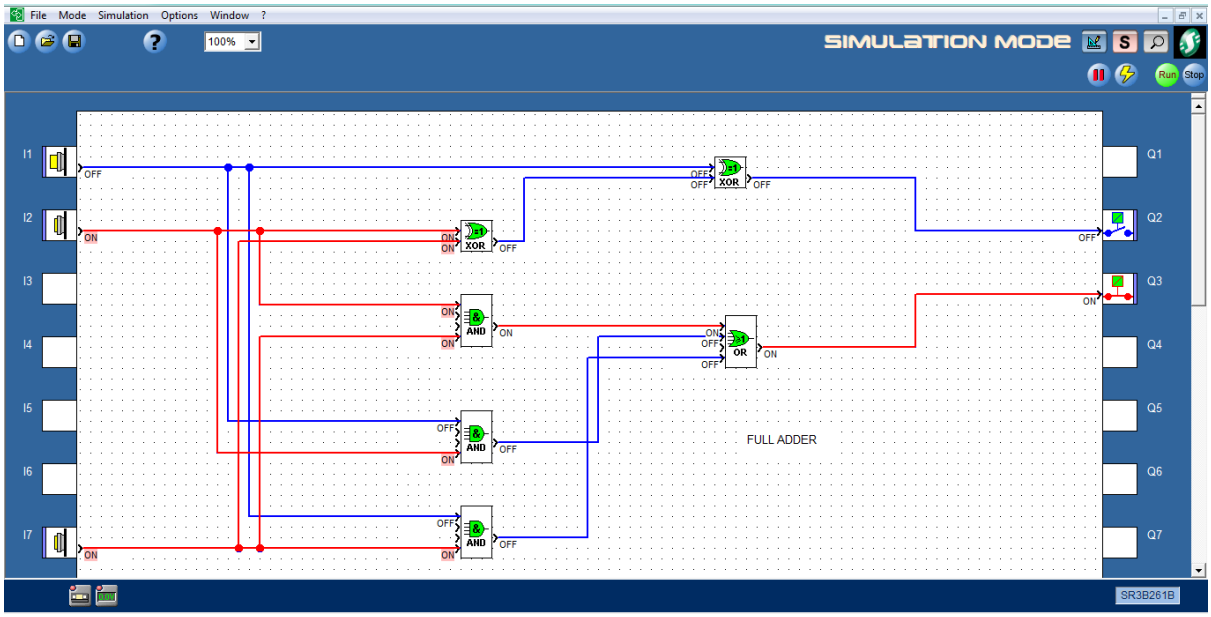


Figure 4.4 Simulation Full Adder

b. Multiplexer and Demultiplexer

Multiplexers in Figure 4.5 has four input using push button and a yellow color selector signal using the push button blue. At the signal selector is used and the data input NOT gate using the AND gate. Output Multiplexer using four input OR gate and relay

contacts. The simulation shows if the second selector push button push button and all the data gives a logic 1, then the input data multiplexer is out on the third data.

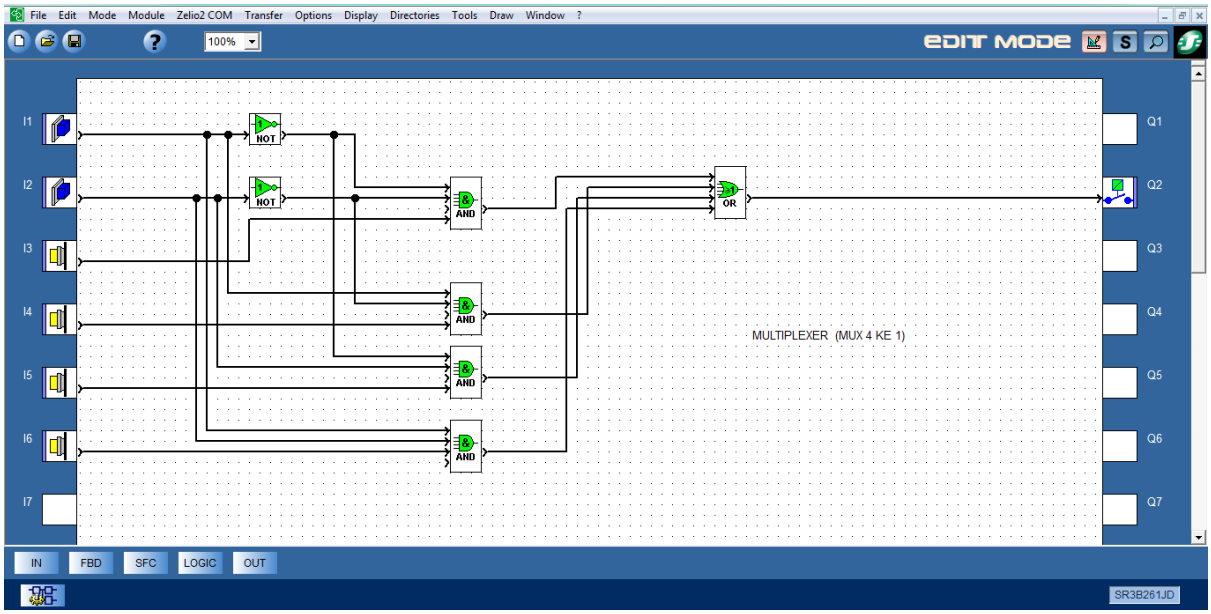


Figure 4.5 Designed by Multiplexer

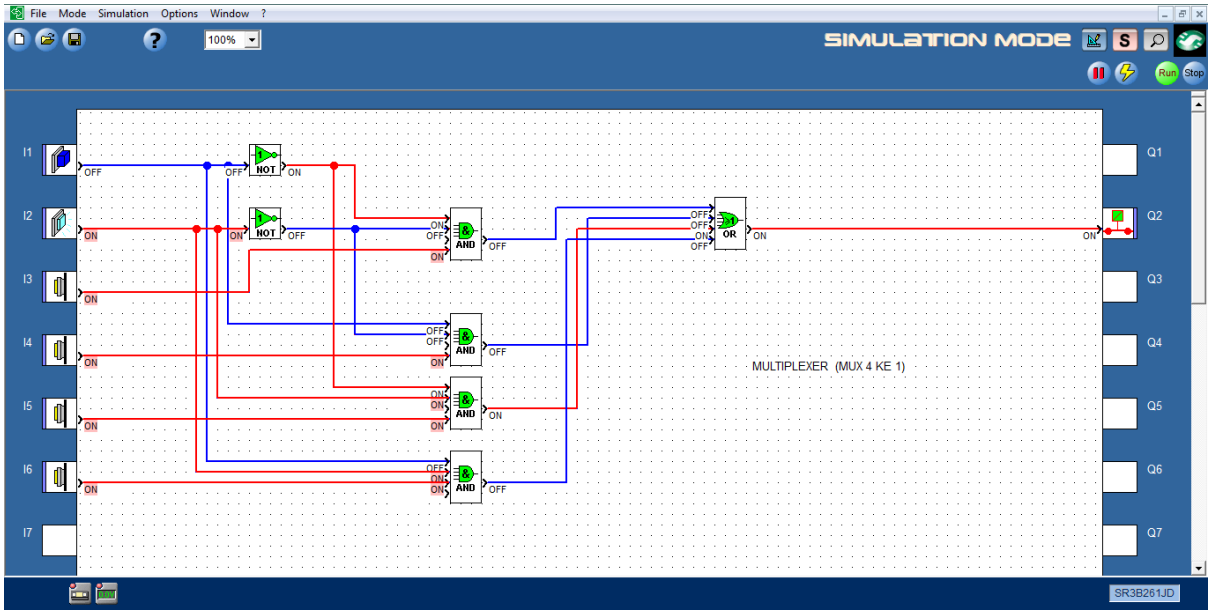


Figure 4.6 Simulation Multiplexer

Because demultiplexer is the opposite of the input multiplexer then only have one data input using push button and signal selector kunimg color using push button blue. Four output demultiplexer (Q) are all using the relay contacts and if the AND gate provides a logic 1 then the relay contacts will close. By the time the signal push button push button selector and the data provide a logic 1, the input data will be passed on the fourth gate of the demultiplexer, while the other three AND gate provides output logic 0 (off).

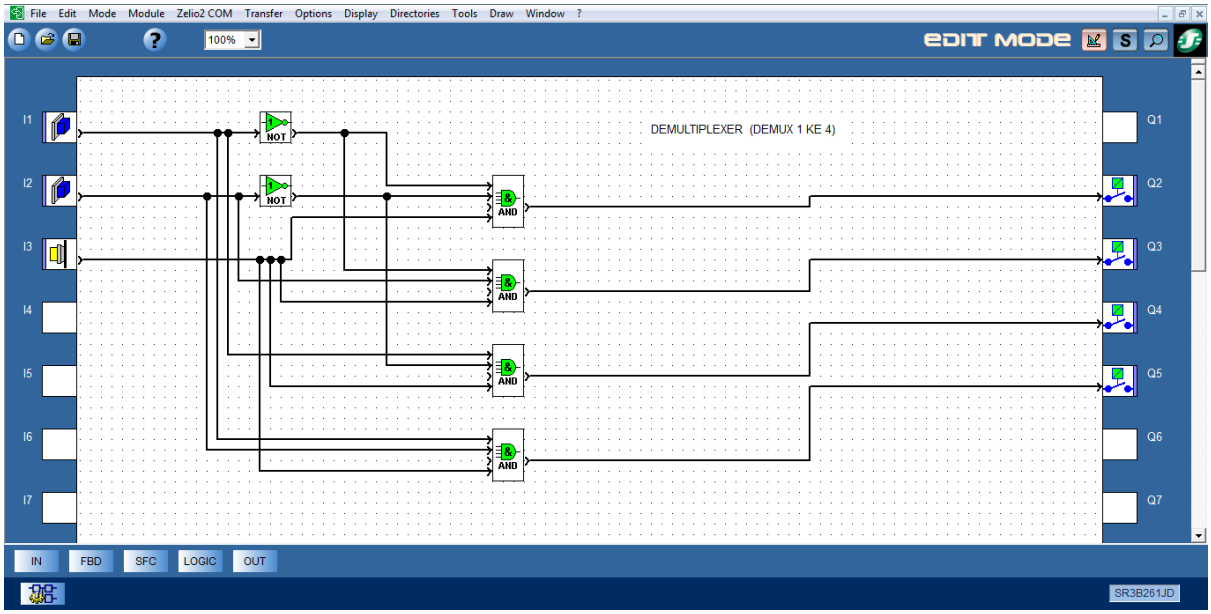
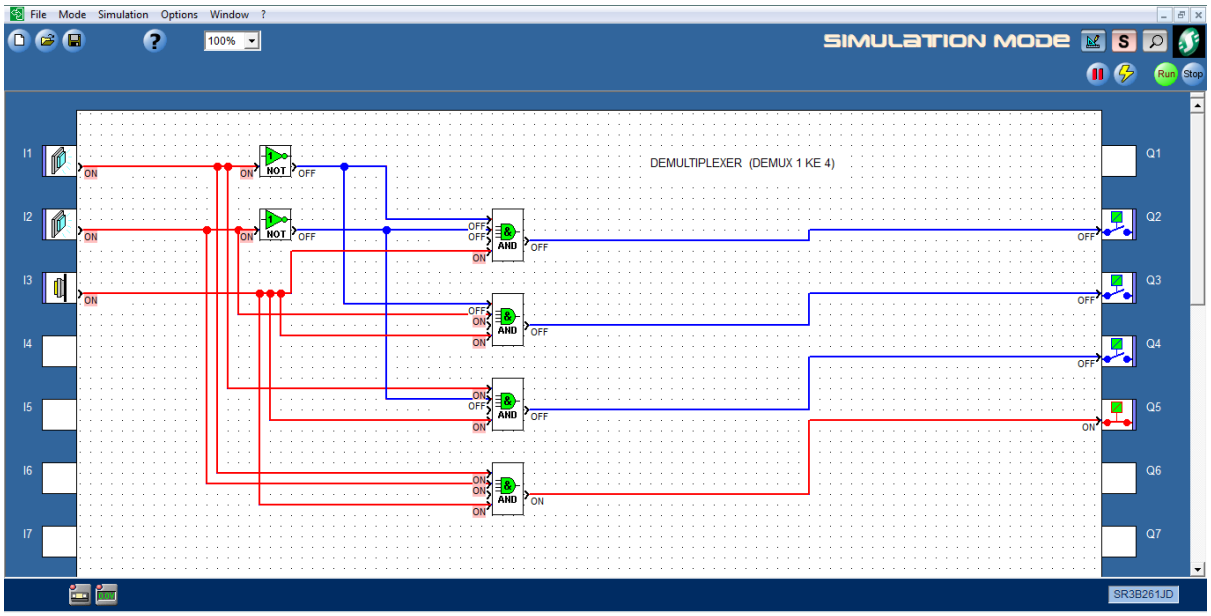


Figure 4.7 Designed by demultiplexer



Gambar 4.8 Simulation Demultiplexer

c. Decoder

In designing Decoder NOT gate takes two and four AND gates, the data input has two inputs with four combinations of binary data. If the binary data 01 which means first off push button and the second button on the push button, then the second gate which will provide a logic 1 at the output (Q).

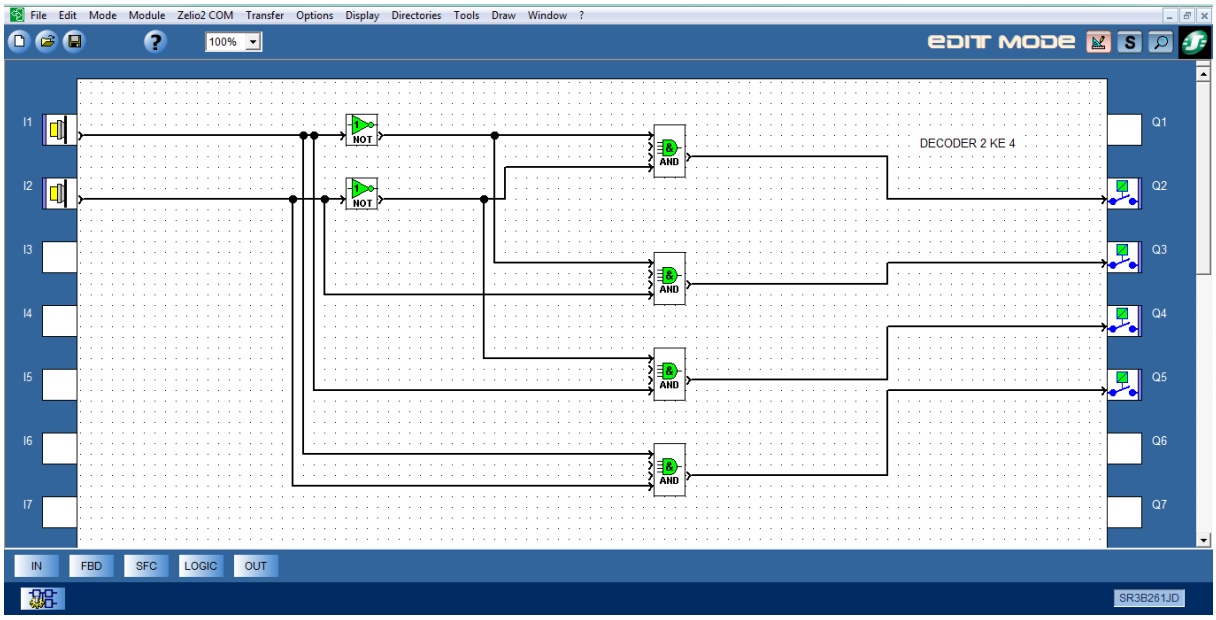


Figure 4.9 Designed by Decoder

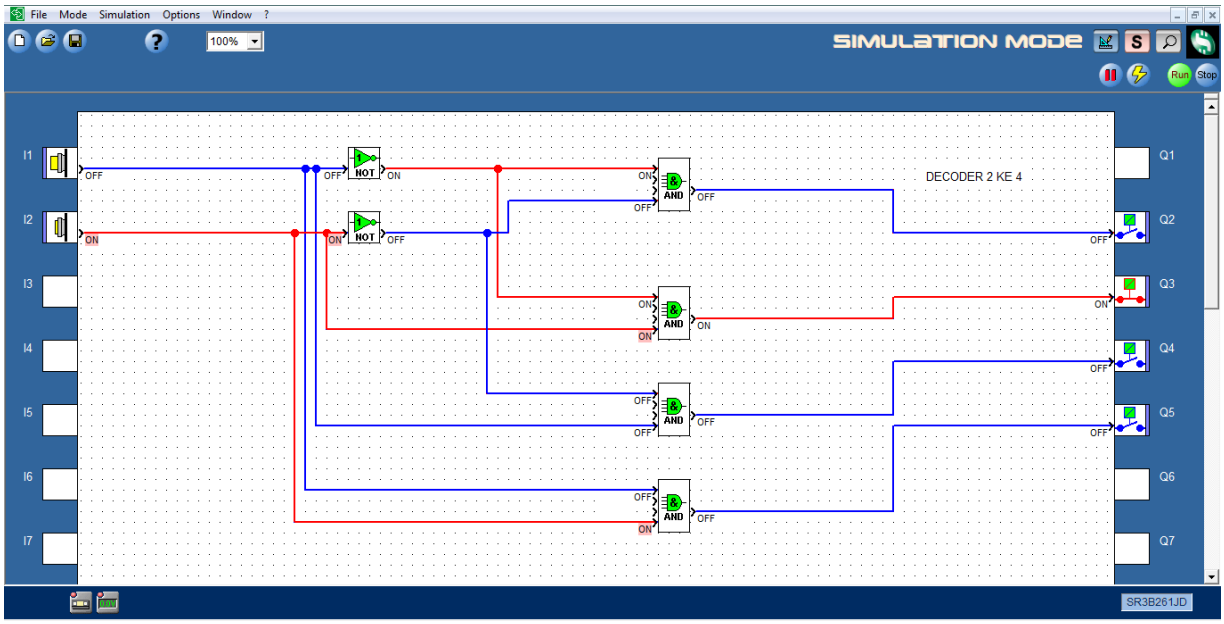


Figure 4.10 Simulation Decoder

d. Water level control circuit

In the design of the water level controllers used four entries which include the stop button (A), the start button (B), upper tank sensor (C), the bottom tank sensor (D). There are two system output electric motor or pump motor (Q1) and indicators (Q2). Table 4.1 shows the input and output of the system design. By using Karnaugh-map then can be generated logic gate circuit design minumum for controlling the water level.

Table 4.1 The design of the water level controllers

INPUT				OUTPUT	
A	**B**	**C**	**D**	**Q1**	Q2

0	0	0	0	0	1
0	0	0	1	0	1
0	0	1	0	0	1
0	0	1	1	0	1
0	1	0	0	0	1
0	1	0	1	0	1
0	1	1	0	0	1
0	1	1	1	0	1
1	0	0	0	0	1
1	0	0	1	1	0
1	0	1	0	0	1
1	0	1	1	0	1
1	1	0	0	0	1
1	1	0	1	1	0
1	1	1	0	0	1
1	1	1	1	0	1

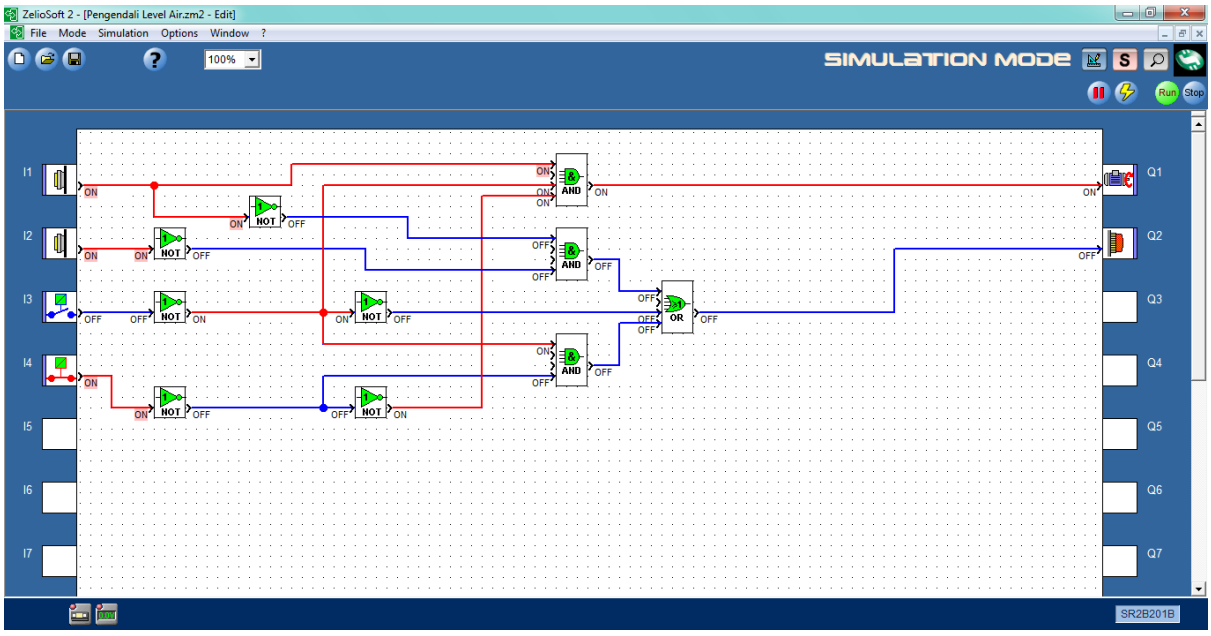


Figure 4.11 Water level controller circuit simulation

From the simulation results seen when both keys in a closed condition and under a closed tank level sensor, the pump motor will work to channel water into the water tank. If the tank above the water level sensor is closed then the motor pump will stop working, because the contents of the water tank is full.

e. Pump Motor Control circuit Hydrant

In the control system of the water in the hydrant pipeline network used three pumps. Electric pump and jockey pump uses a three-phase electric motor and the diesel pump did not use three-phase electric motor, but using diesel propulsion engine. The amount of capacity pumps are used depending on the length of the pipeline network hydrant installation.

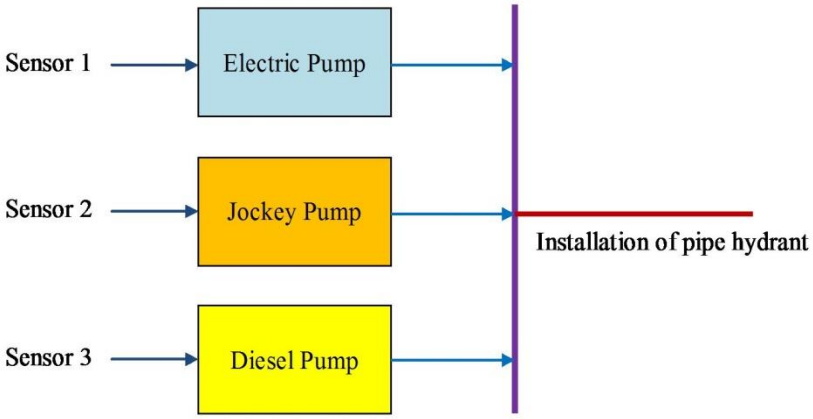


Figure 4.12 Diagram hydrant control systems

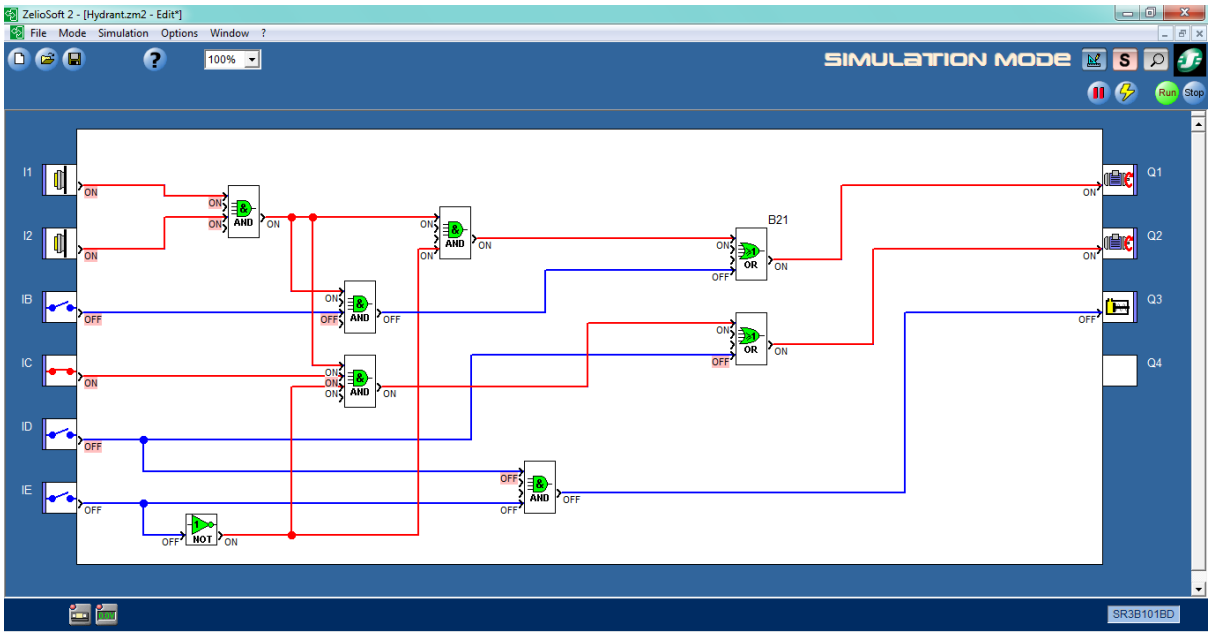


Figure 4.13 Simulation of control systems of the building during a fire hydrant

At the time of normal circumstances, jockey pump motors will work to stabilize the water pressure in hydrant installation network. In this case the second sensor (pressure sensor) will provide feedback or information on the controller to regulate the working jockey pump motors. If the water pressure in the pipeline network hydrant installations are not able to overcome by jockey pump, the pressure sensor will work to give the order for electric motors pump works to achieve the desired water pressure. In the event of a fire, the heat sensors and smoke sensors will be giving orders to the controller so that the motor electric

pump works, so that the process can be carried out by the extinguishing the fire hydrant box. Sensor 1 is a pressure sensor, fire sensor, and smoke sensors. In the event of a power outage caused by a fire, the diesel pump will take over the process of extinguishing the fire of the electric pump. This is done by a third sensor (sensor voltage).

Conclusion

First, Zelio Soft 2 is also used to make the program ladder diagram (LD) can also be used to create the design of digital circuits consisting of a combination of basic logic gates, Half Adder, Full Adder, multiplexer, demultiplexer, and decoders using the program function block (FBD).

Second, to implement the results of the combination of digital circuit design needed Zelio logic devices with a choice of the type and source voltage as needed.

Third, the simulation has been done on digital circuits using a combination of FBD program Zelio Soft 2 to facilitate the analysis.

Fourth, Zelio Soft 2 with FBD option can be used to design a combination of logic gates on the water level controllers and motor controllers hydrant pump.

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